Patented Application

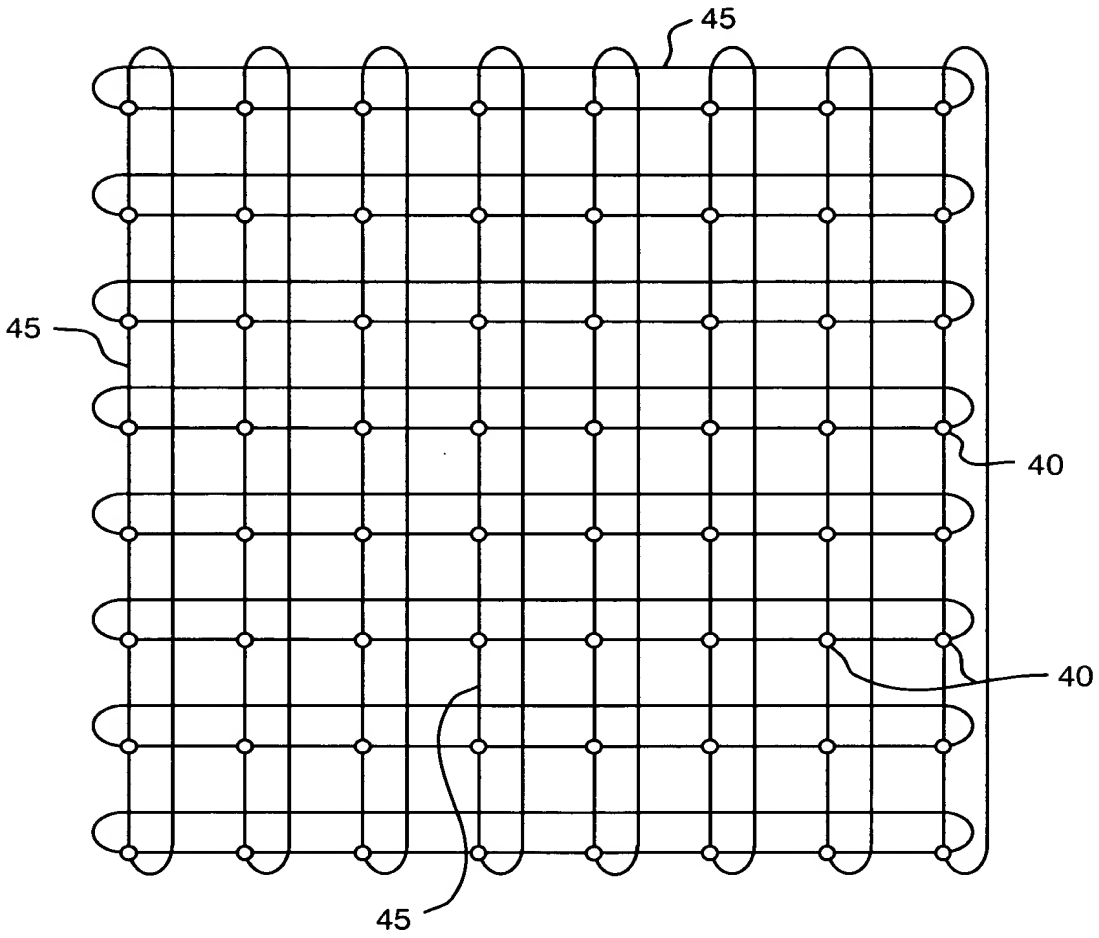

FIG. 1

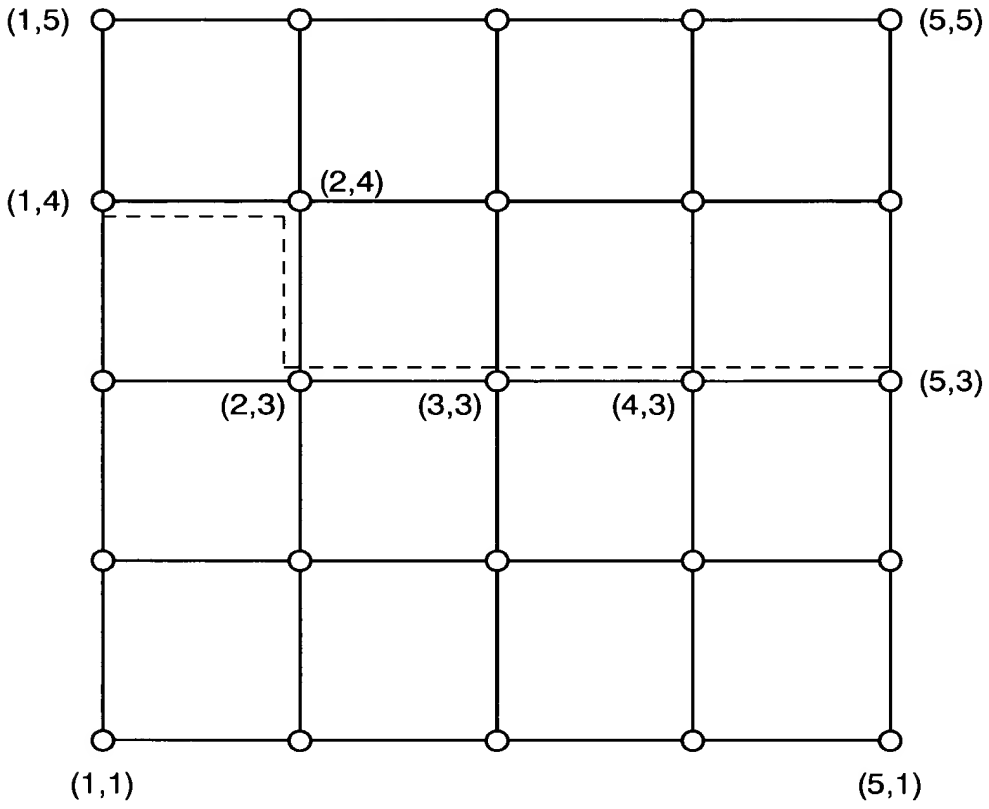

FIG. 2

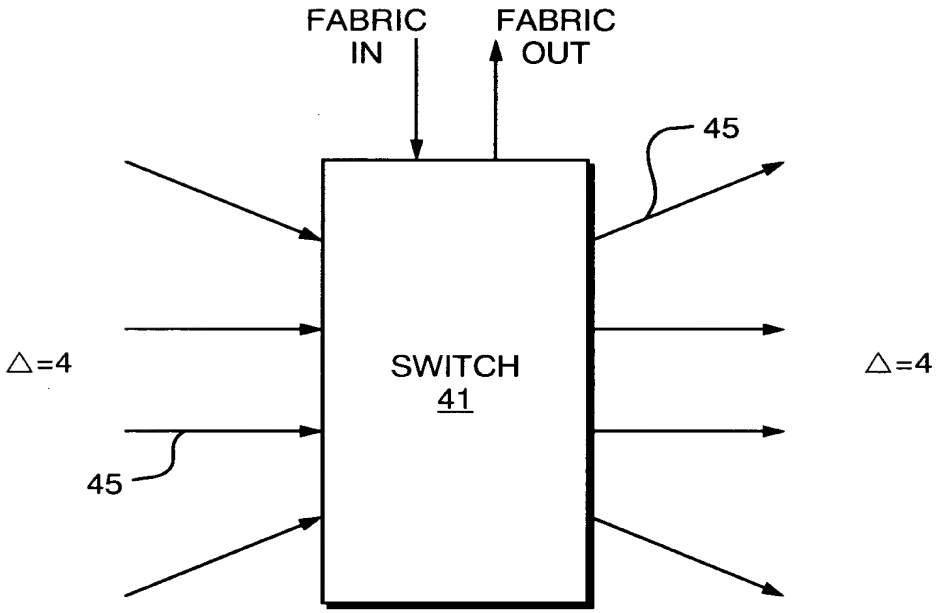

FIG. 3

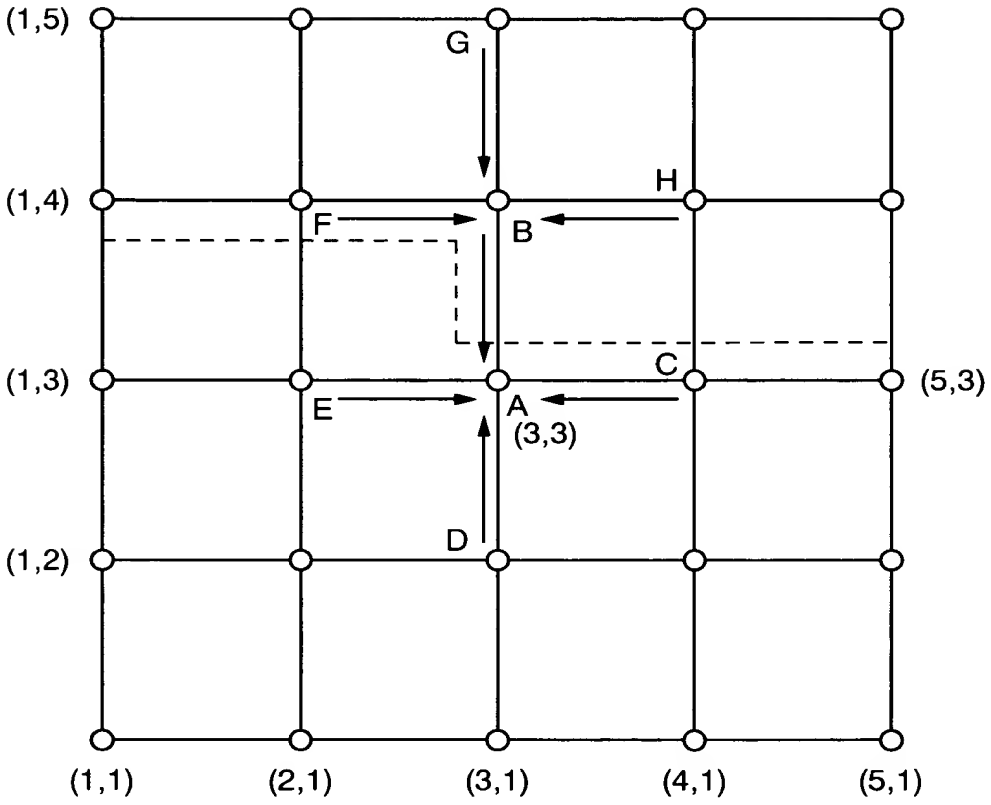

FIG. 4

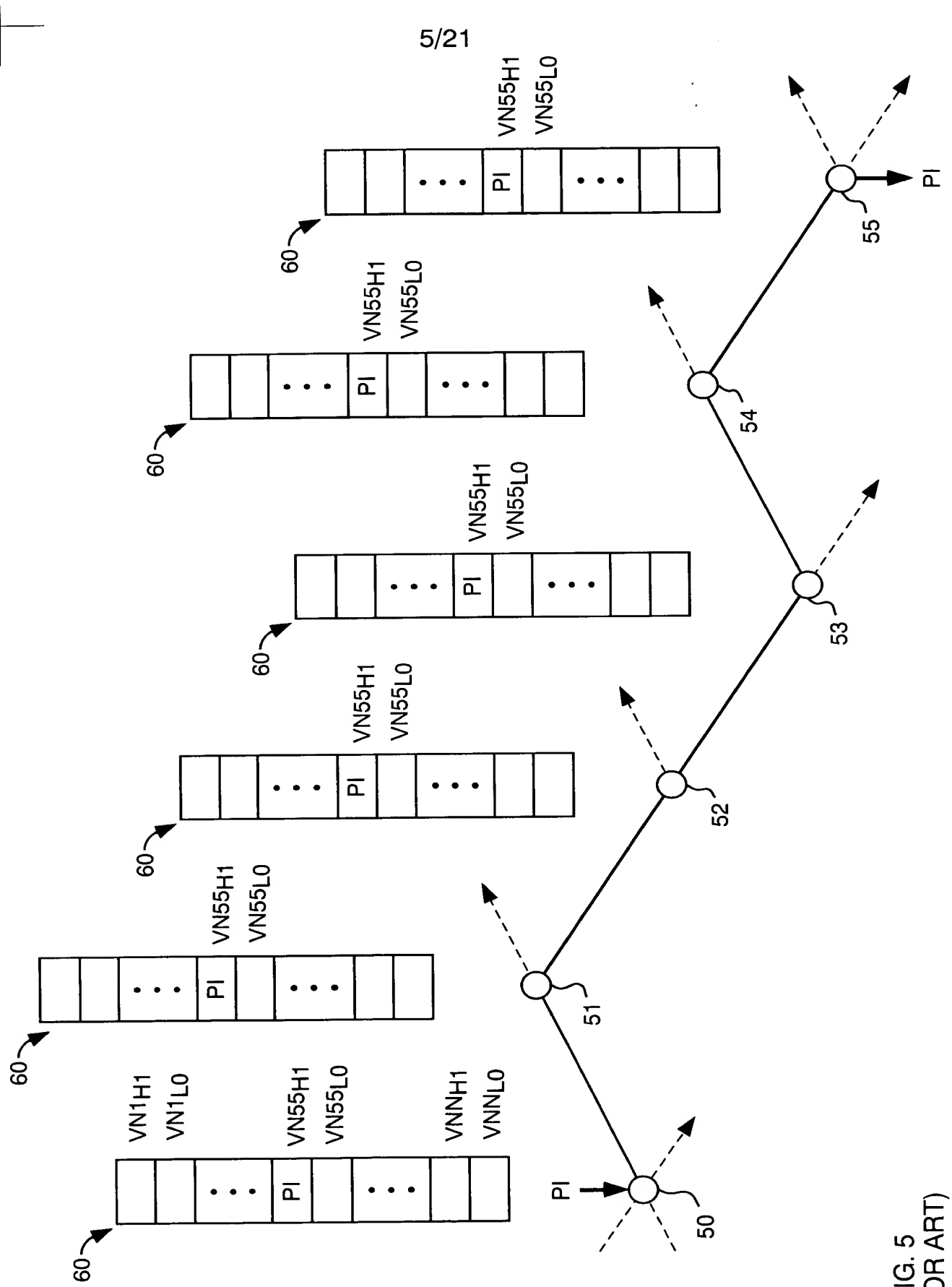

FIG. 5
(PRIOR ART)

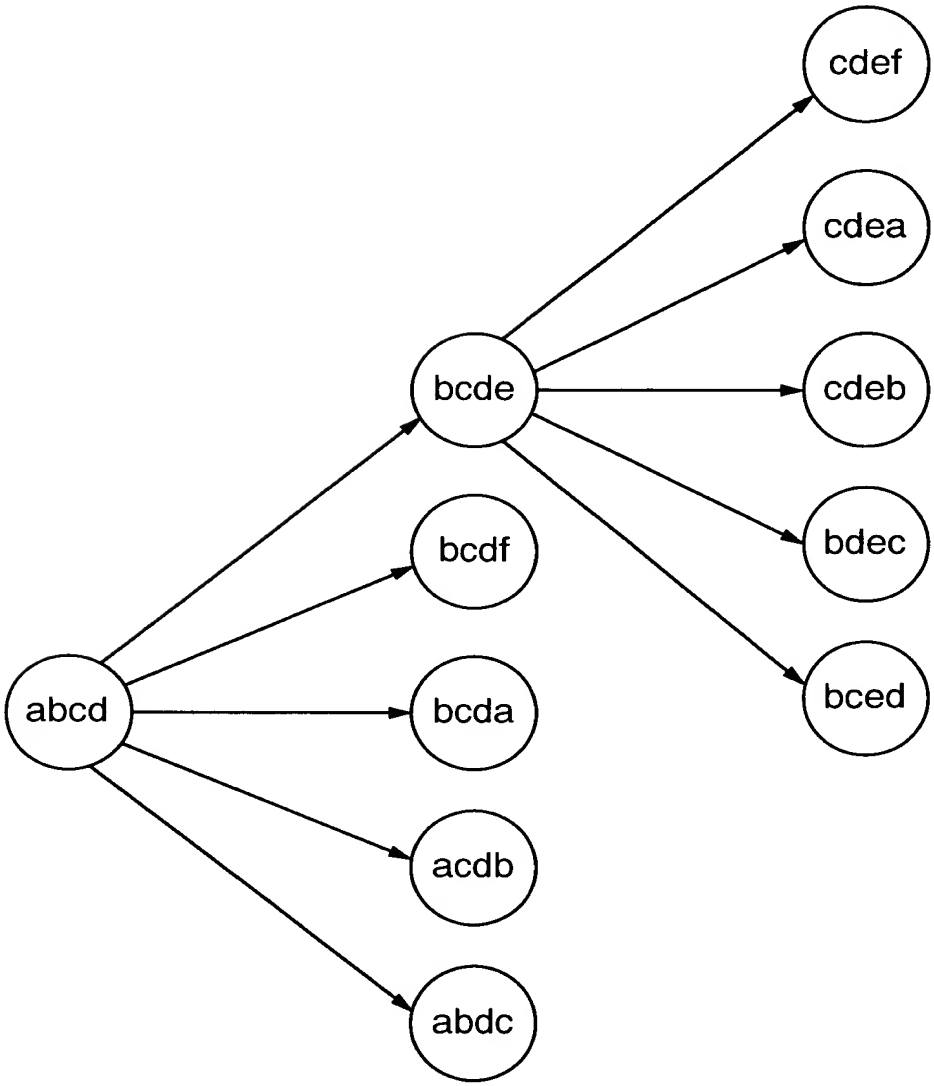

FIG. 6A

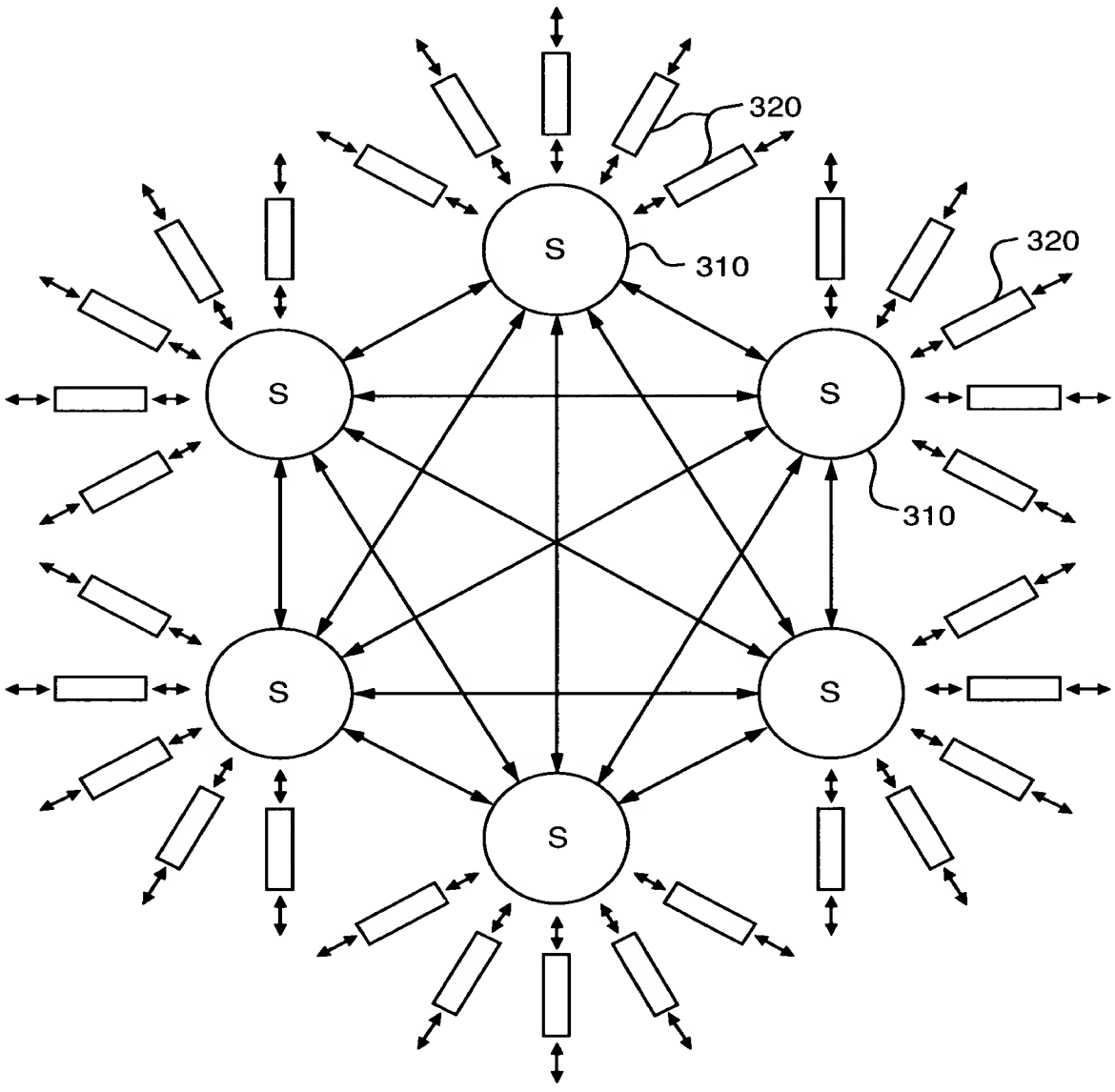

FIG. 6B

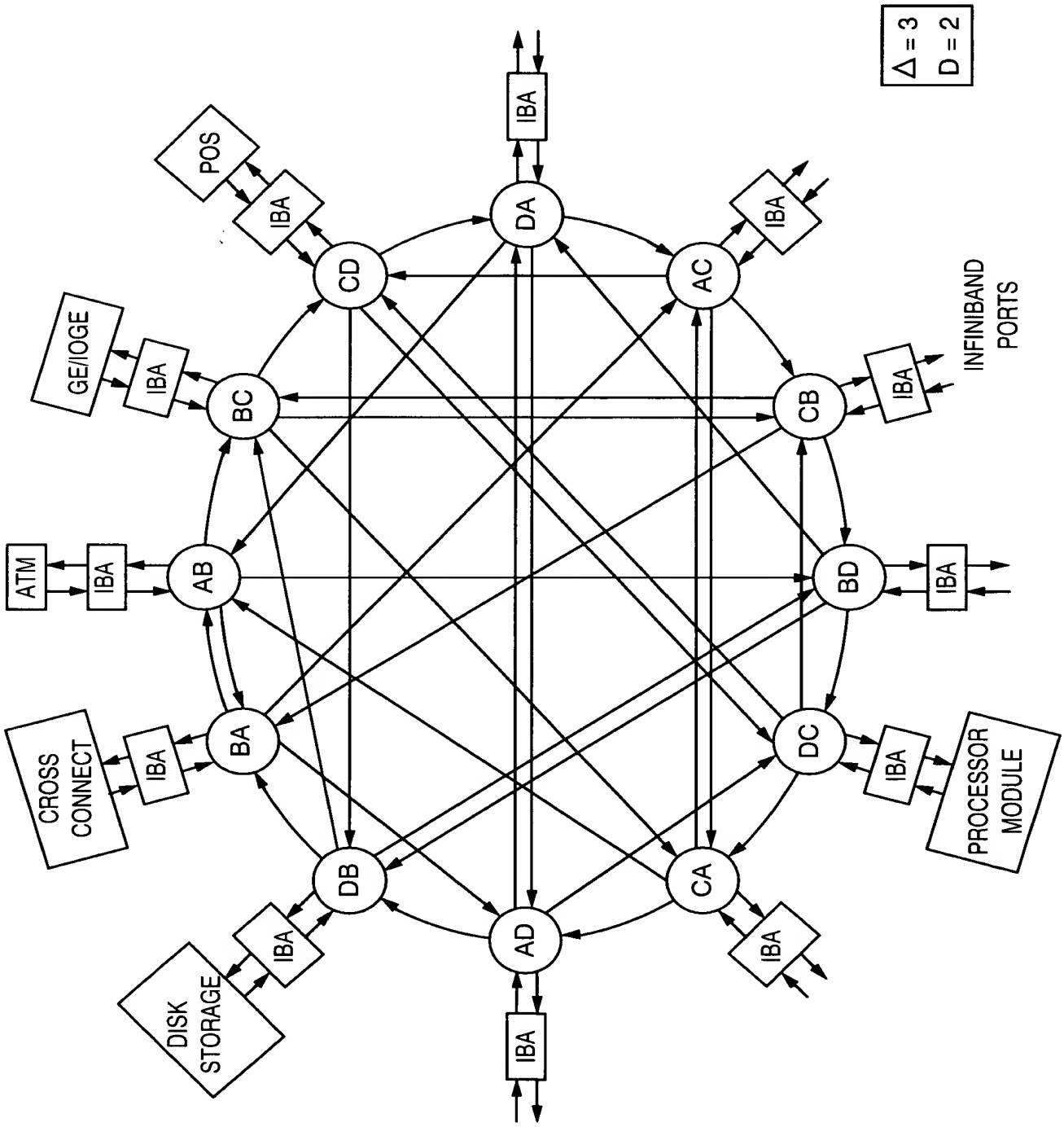
Δ = 3
D = 2
INFINIBAND PORTS
DA
AC
CB
BD
DC
CA
AD
DB
BA
AB
CD
BC
IBA
POS
GE/IOGE
ATM
CROSS CONNECT
DISK STORAGE
PROCESSOR MODULE

FIG. 7A

09866335 - 030401

AB	AC	AD
AB → BC	AC → CB	AD → DB
AB → BD	AC → CD	AD → DC
AB → BA	AC → CA	AD → DA

BA	BC	BD
BA → AC	BC → CD	BD → DA
BA → AD	BC → CA	BD → DC
BA → AB	BC → CB	BD → DB

CA	CB	CD
CA → AB	CB → BD	CD → DA
CA → AD	CB → BA	CD → DB
CA → AC	CB → BC	CD → DC

DA	DB	DC
DA → AB	DB → BA	DC → CA
DA → AC	DB → BC	DC → CB
DA → AD	DB → BD	DC → CD

FIG. 7B

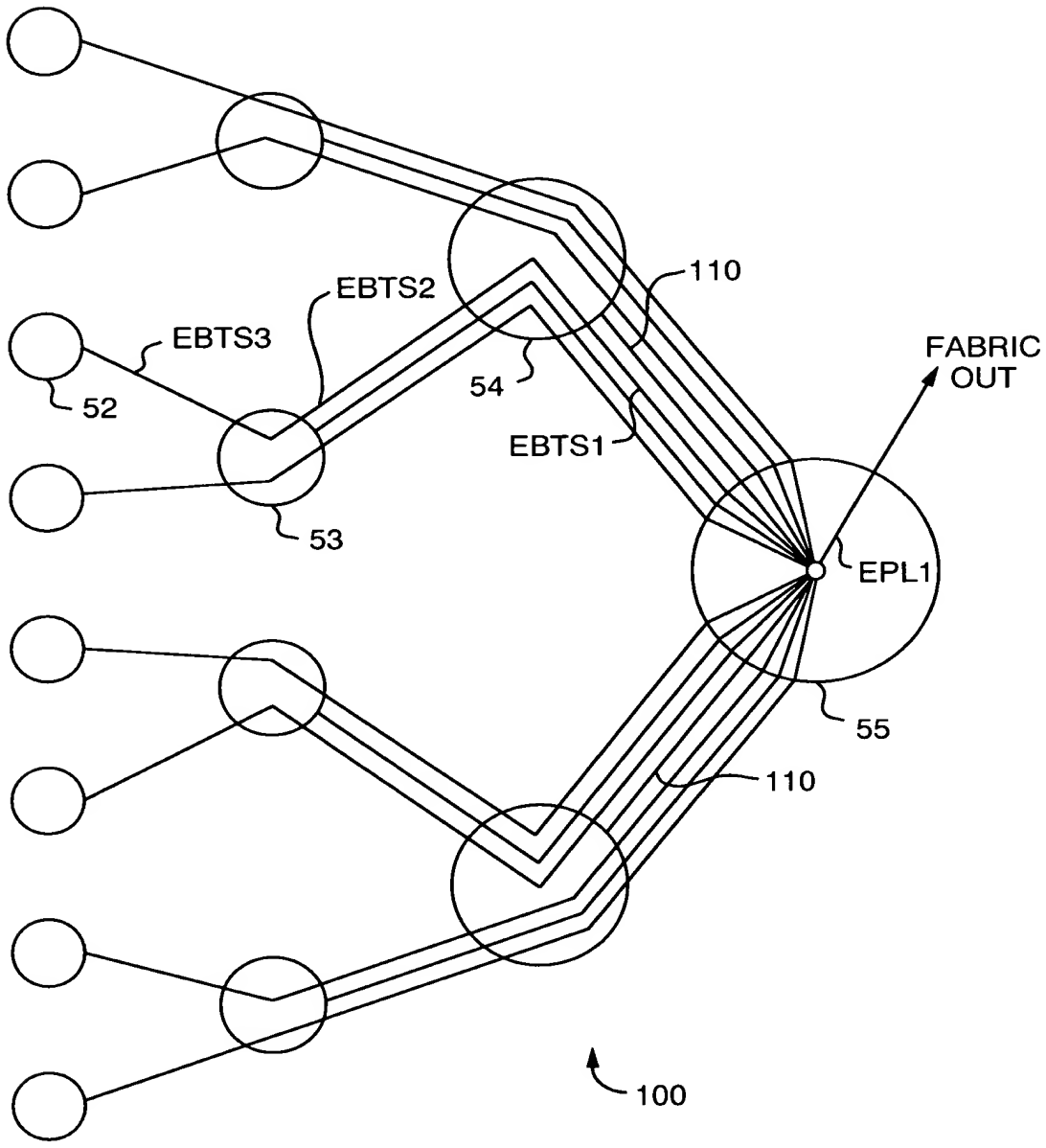

FIG. 8A

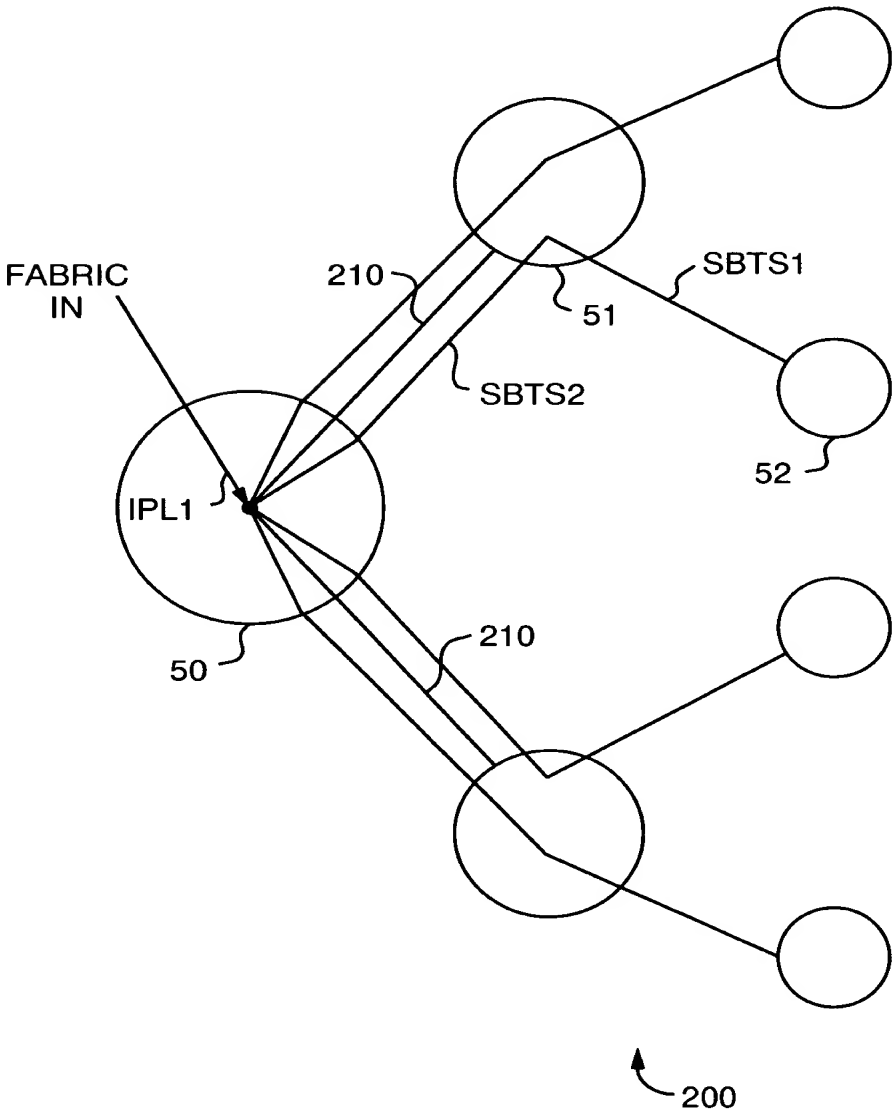

FIG. 8B

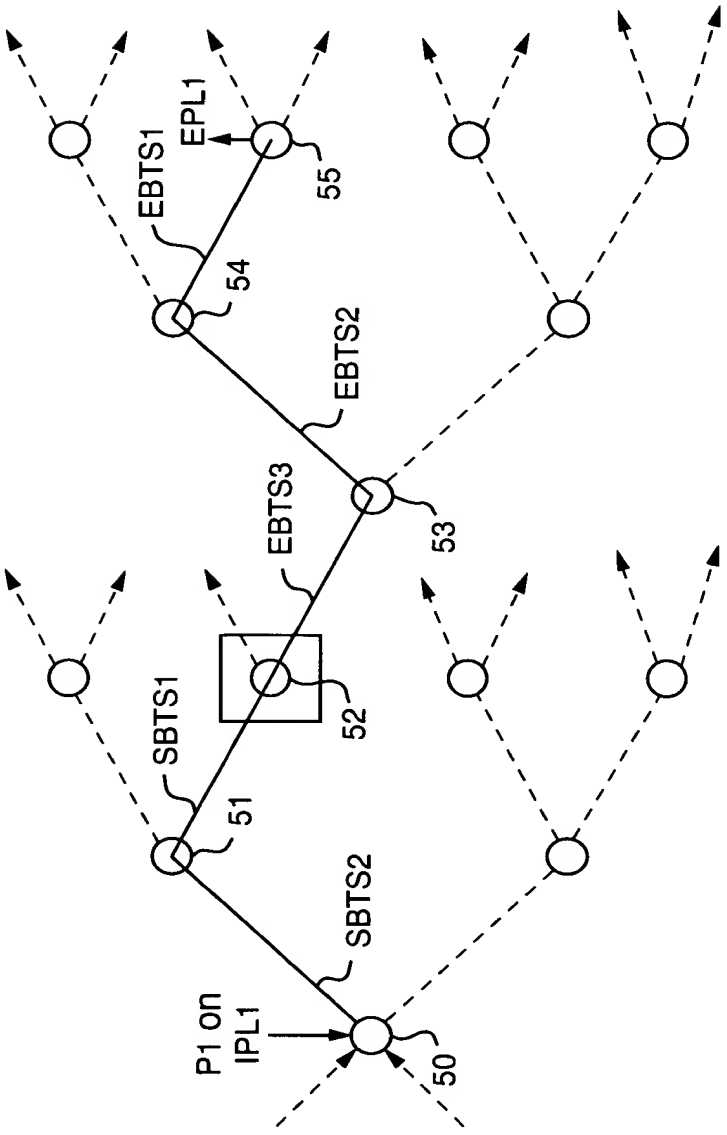

FIG. 9

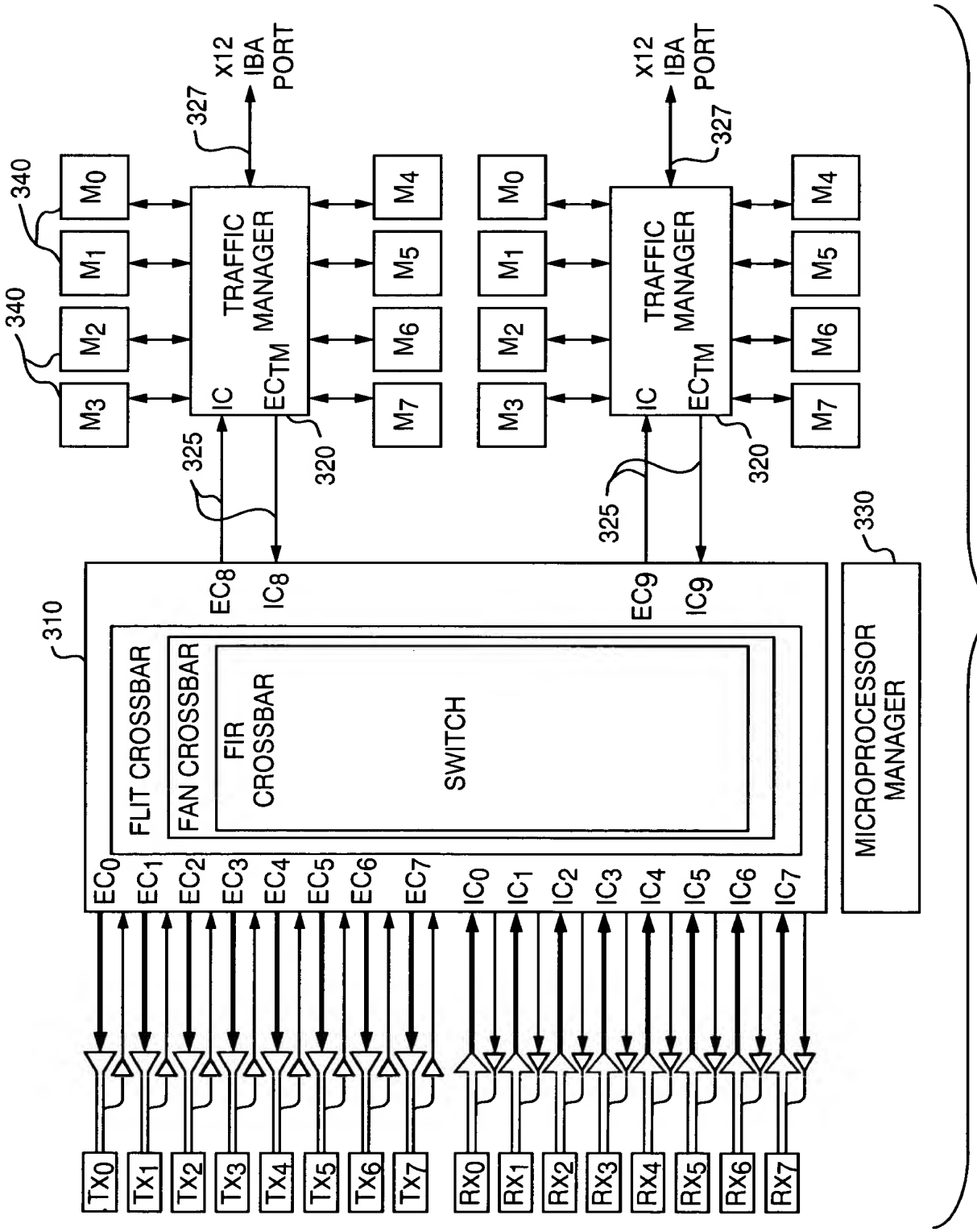
X12 IBA PORT
327
340
M0
M1
M2
M3
TRAFFIC MANAGER
IC
ECTM
M4
M5
M6
M7
325
320
310
FLIT CROSSBAR
FAN CROSSBAR
FIR CROSSBAR
SWITCH
EC0
EC1
EC2
EC3
EC4
EC5
EC6
EC7
EC8
IC8
EC9
IC9
IC0
IC1
IC2
IC3
IC4
IC5
IC6
IC7
330
MICROPROCESSOR MANAGER
TX0
TX1
TX2
TX3
TX4
TX5
TX6
TX7
RX0
RX1
RX2
RX3
RX4
RX5
RX6
RX7

FIG. 10

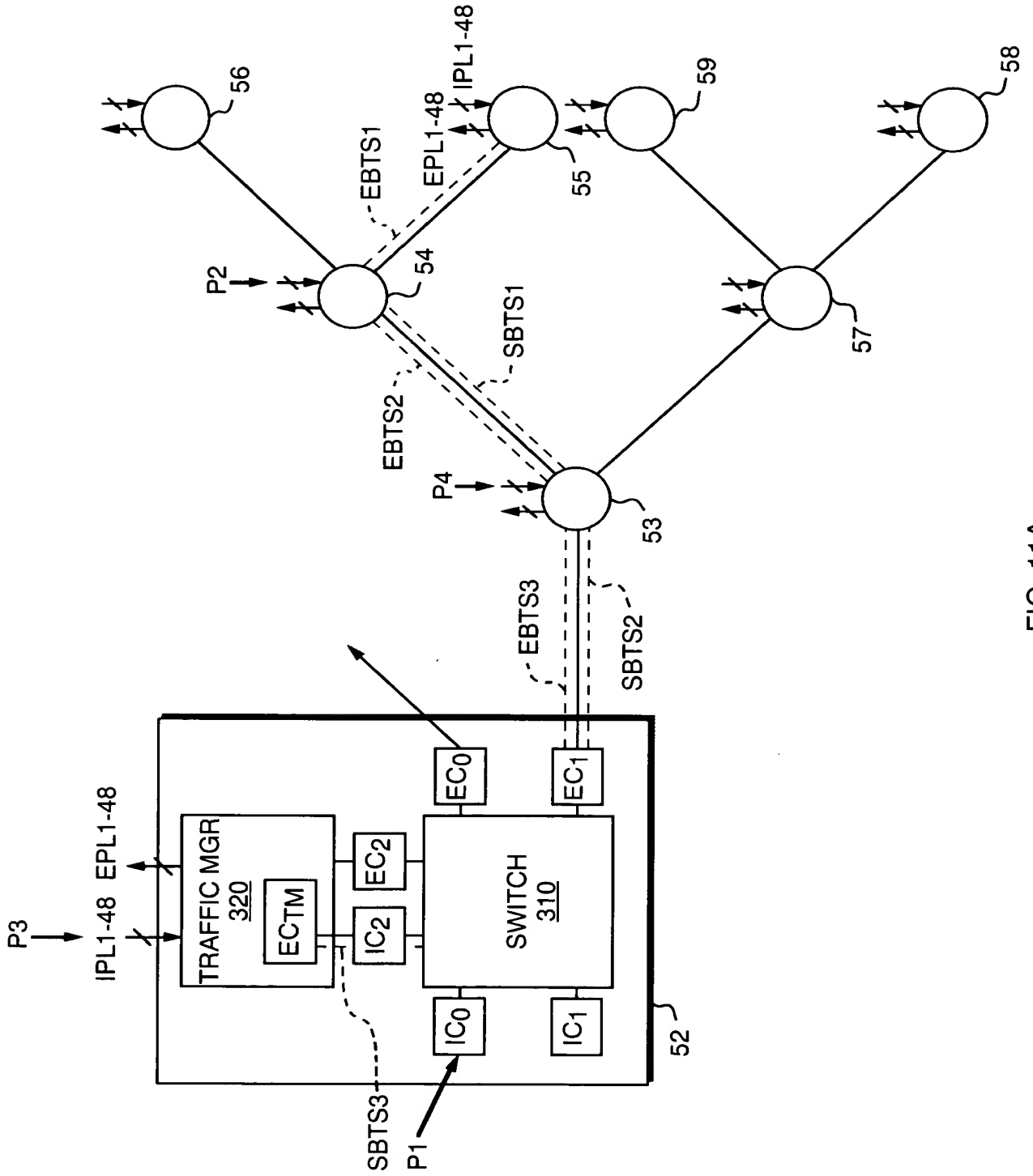
56
IPL1-48
EPL1-48
EBTS1
55
59
58
P2
54
SBTS1
57
EBTS2
P4
53
EBTS3
SBTS2
EC0
EC1
P3
IPL1-48 EPL1-48
TRAFFIC MGR
320
ECTM
EC2
IC2
SWITCH
310
IC0
IC1
52
SBTS3
P1

FIG. 11A

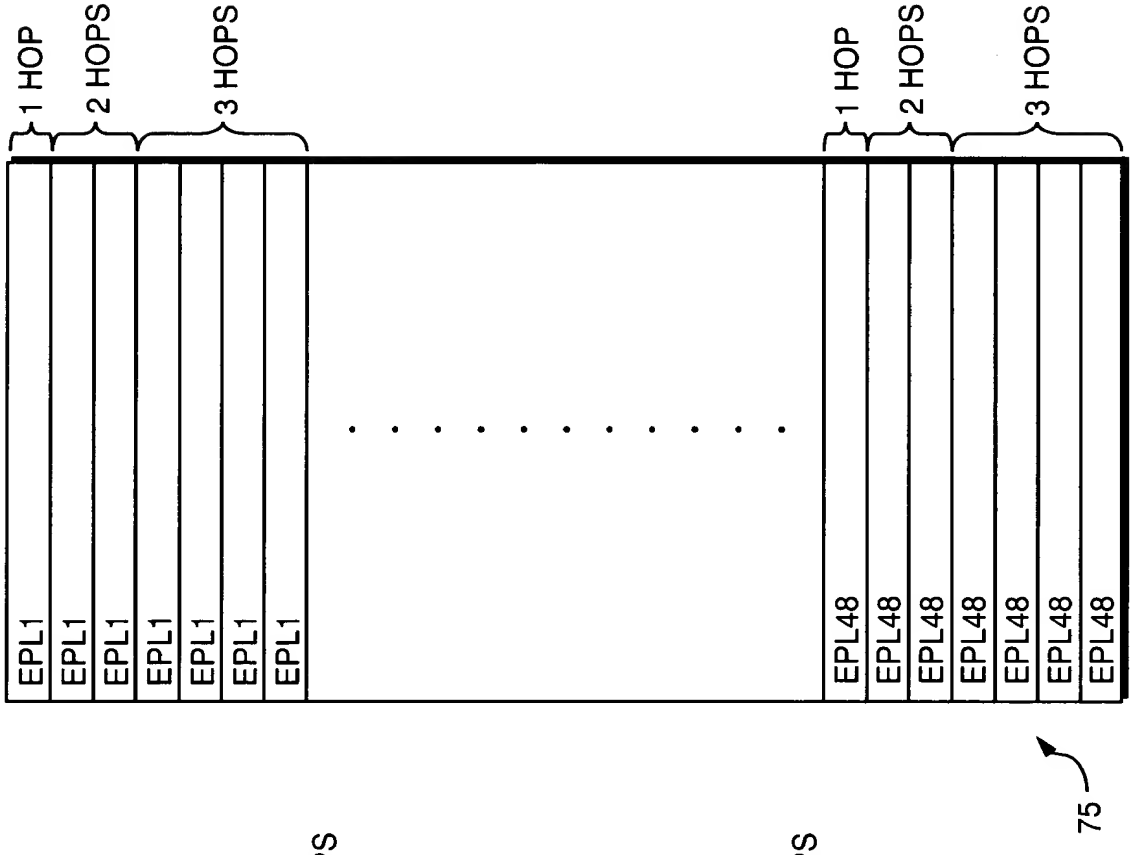

FIG. 11C

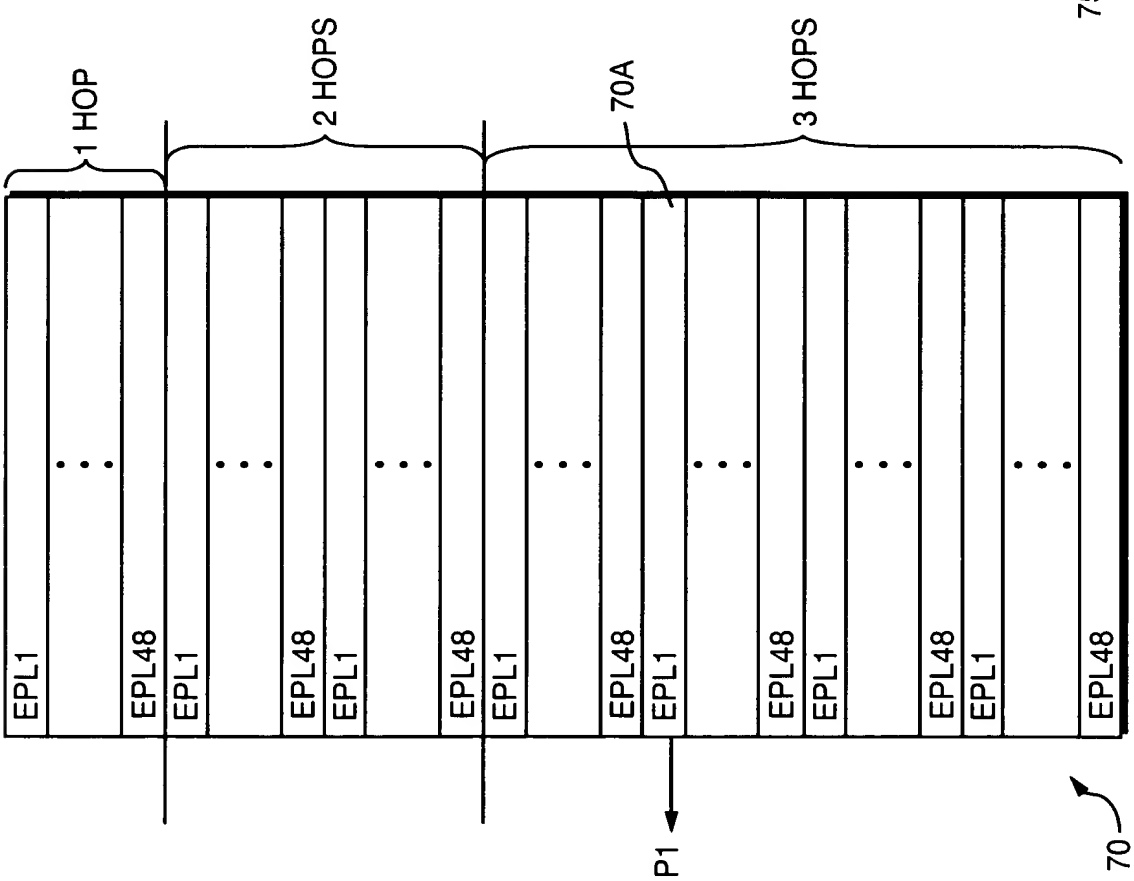

FIG. 11B

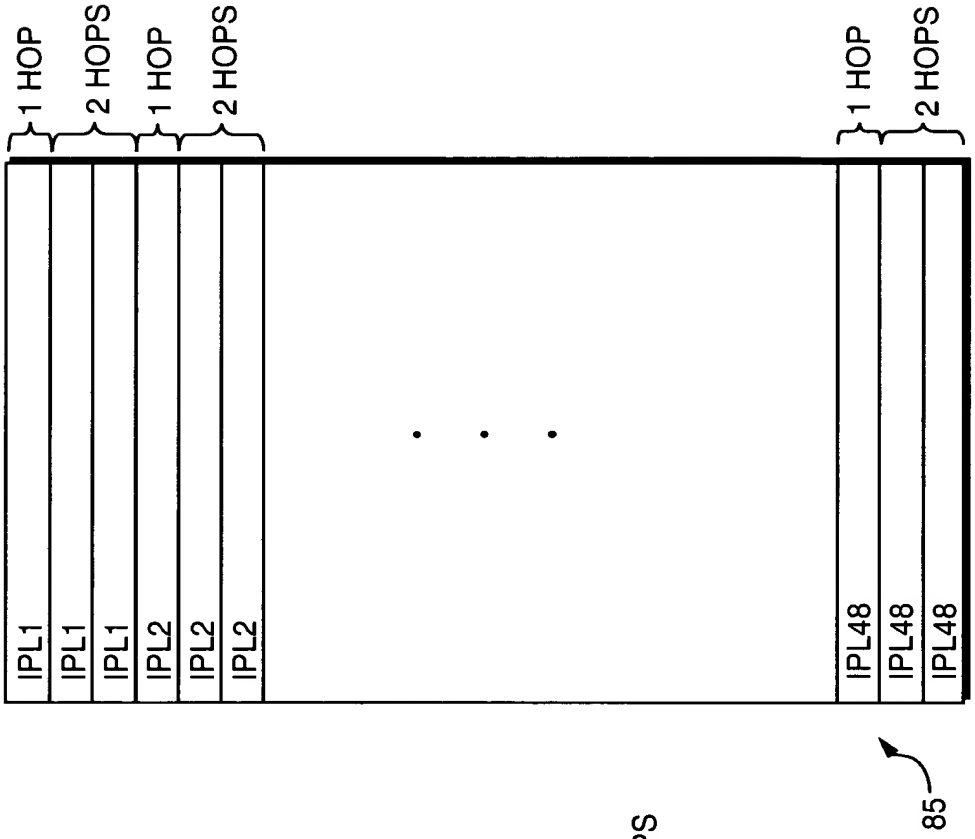

FIG. 11E

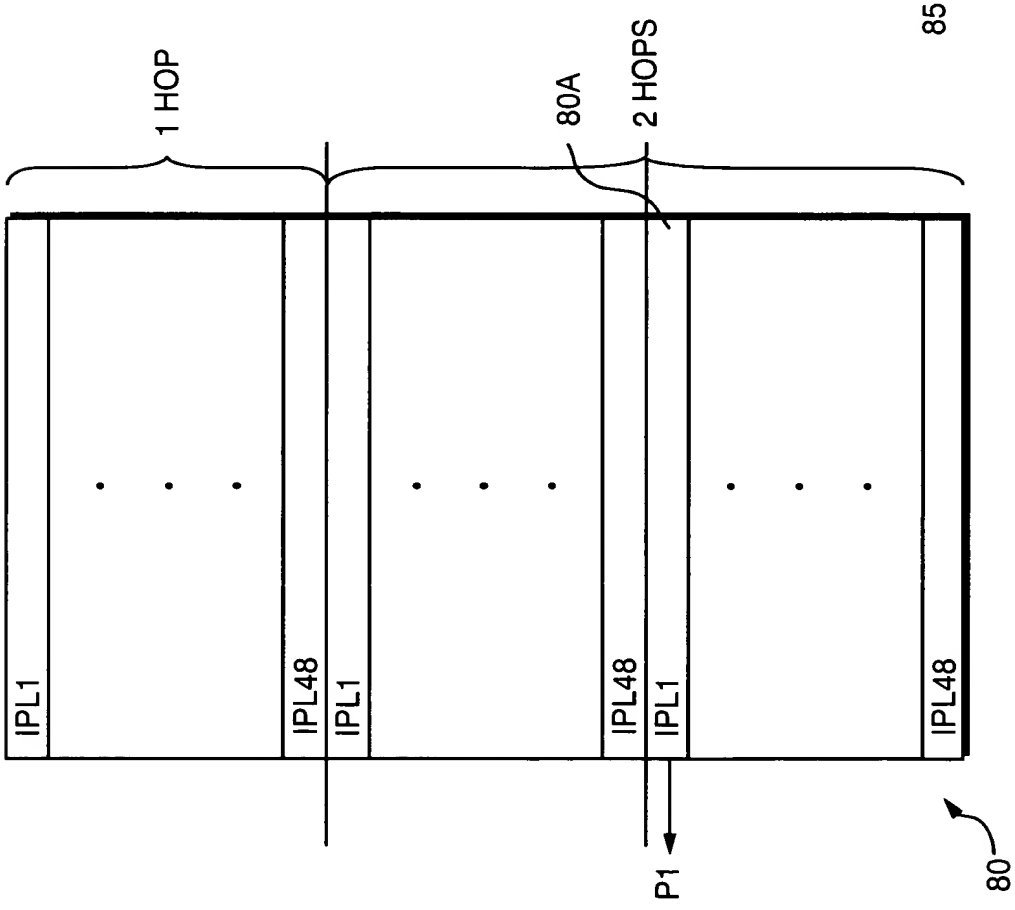

FIG. 11D

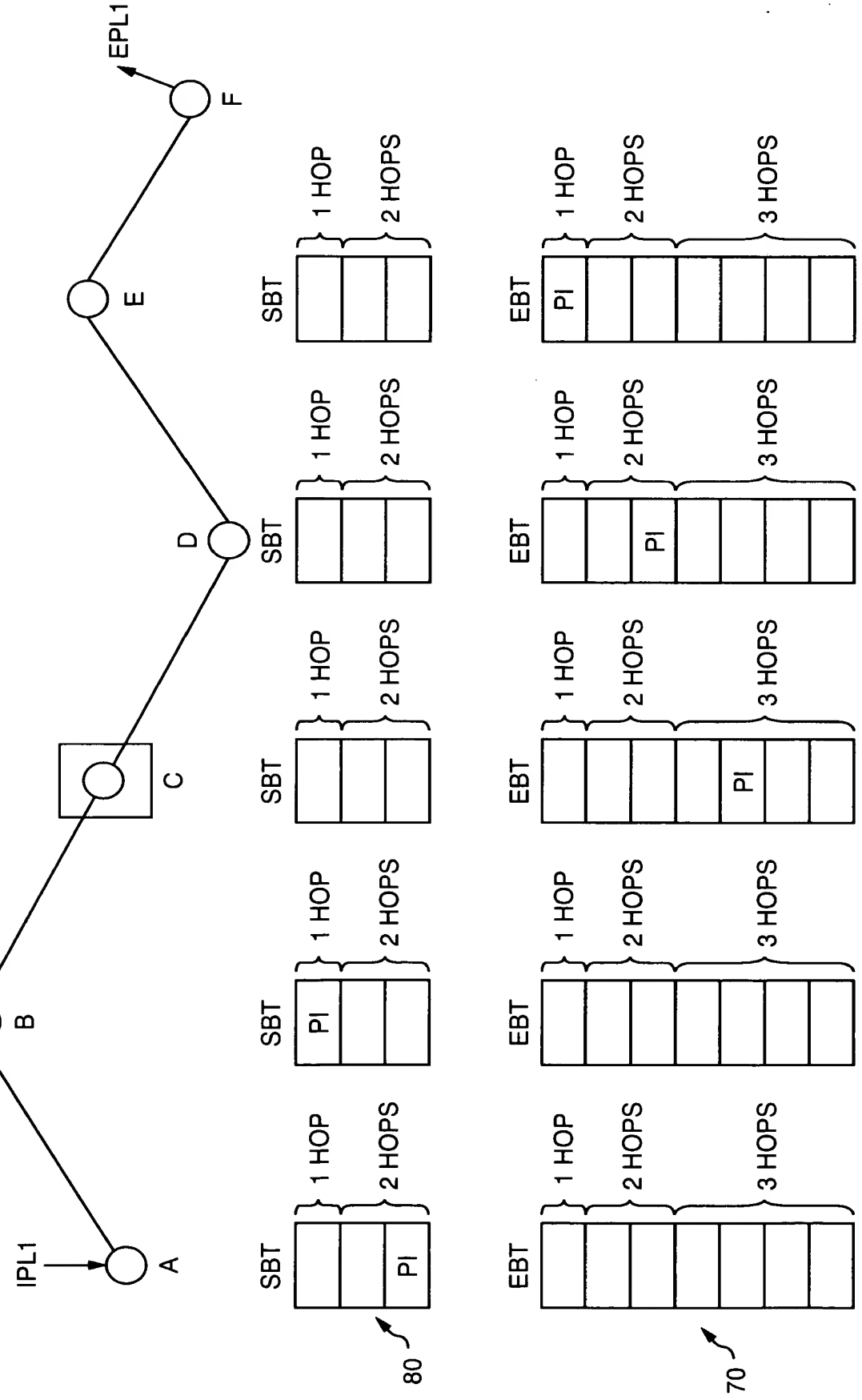

FIG. 11F

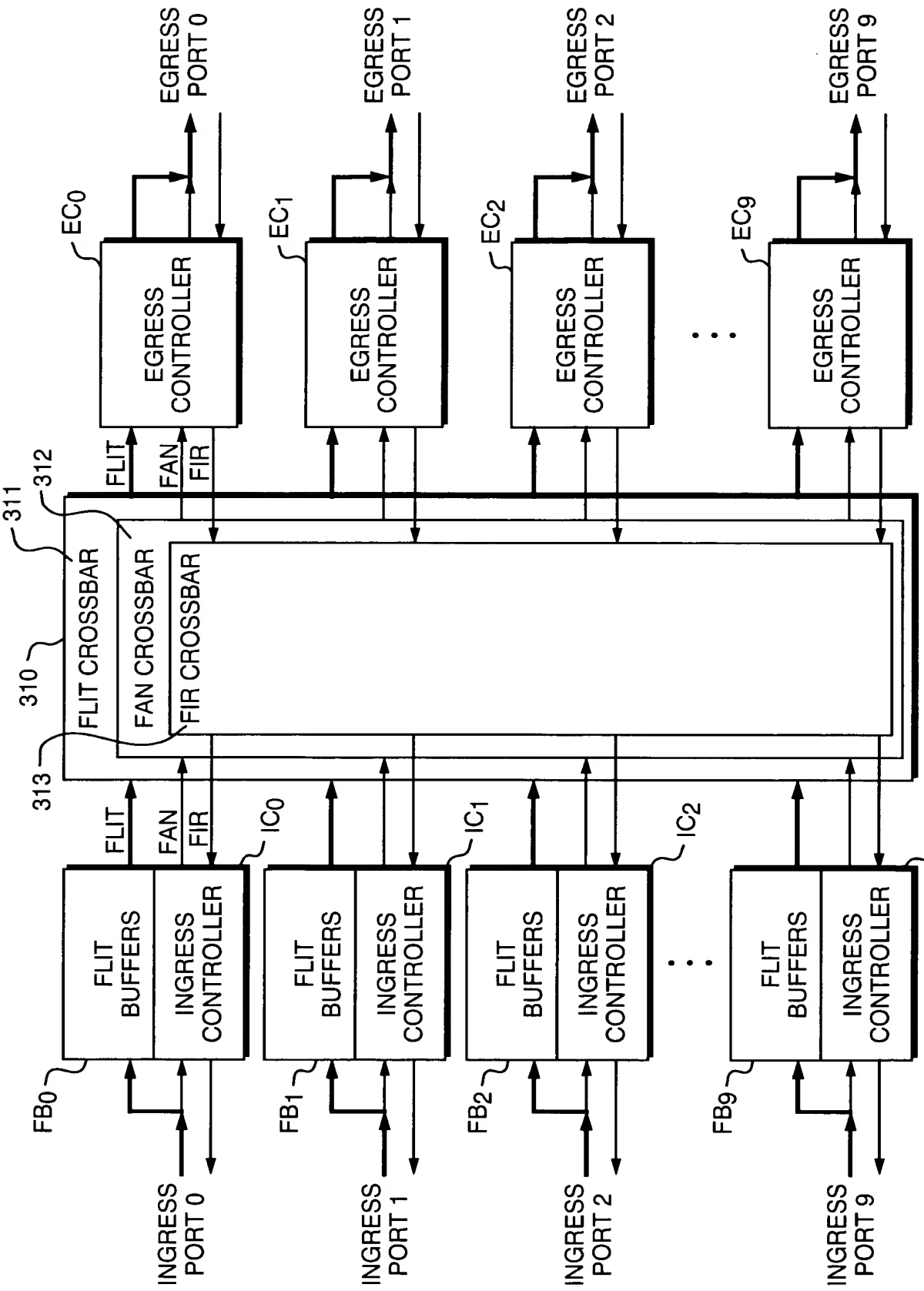
EGRESS PORT 0
EGRESS PORT 1
EGRESS PORT 2
EGRESS PORT 9
EC0
EC1
EC2
EC9
EGRESS CONTROLLER
FLIT
FAN
FIR
311
312
310
313
FLIT CROSSBAR
FAN CROSSBAR
FIR CROSSBAR
IC0
IC1
IC2
IC9
FLIT BUFFERS
INGRESS CONTROLLER
FB0
FB1
FB2
FB9
INGRESS PORT 0
INGRESS PORT 1
INGRESS PORT 2
INGRESS PORT 9

FIG. 12

CONTROL STRUCTURE	SIZE (IN BITS)	DESCRIPTION
IngressPacketState	1280x35=44,800	EACH IngressPacketState STRUCTURE MANAGES THE STORAGE OF A PARTIALLY RECEIVED PACKET ON ONE OF THE INGRESS PORTS.
EgressLaneState	(128x30=3,480)	EACH EgressLaneState STRUCTURE SUPPLIES INFORMATION USED TO PROCESS RECEIVED CREDITS.
AvailableEgressLane	(128x1)	EACH FLAG INDICATES THAT A PARTICULAR LANE IS AVAILABLE OR IN USE.
FanState	(512x44=22,528)	EACH FanState STRUCTURE HOLDS ONE FAN WAITING TO BE CONVERTED INTO A FIR AND POINTERS WHICH ALLOW CREATING A LINKED LIST OF PACKETS WAITING ON A PARTICULAR CHANNEL AND A LINKED LIST OF FANs COMPRISING A PARTICULAR PACKET.
AvailableFanState	(512x1)	EACH FLAG INDICATES THAT A PARTICULAR LOCAL FANSTATE STRUCTURE IS AVAILABLE OR IN USE.
WaitingForLanes	(2928x1)	EACH FLAG INDICATES THAT A PARTICULAR TUNNEL SEGMENT HAS A PACKET READY TO BE ASSIGNED TO A LANE AS SOON AS ONE BECOMES AVAILABLE.
WaitingForFSM	(2928x1)	EACH FLAG INDICATES THAT A PARTICULAR CHANNEL HAS A FAN READY TO BE CONVERTED INTO A FIR AS SOON AS THE EgressController HAS BANDWIDTH AVAILABLE TO PERFORM THE CONVERSION.
WaitingForFirFifo	(2304x1)	EACH FLAG INDICATES THAT A PARTICULAR LANE HAS A FAN READY TO CONVERT INTO A FIR AS SOON AS ROOM IN THE FIR FIFO BECOMES NON-FULL.
SegmentPointer	(2938x13=38,194)	EACH SegmentPointer POINTS TO A QUEUE OF PACKETS WAITING ON A TUNNEL SEGMENT.

FIG. 13

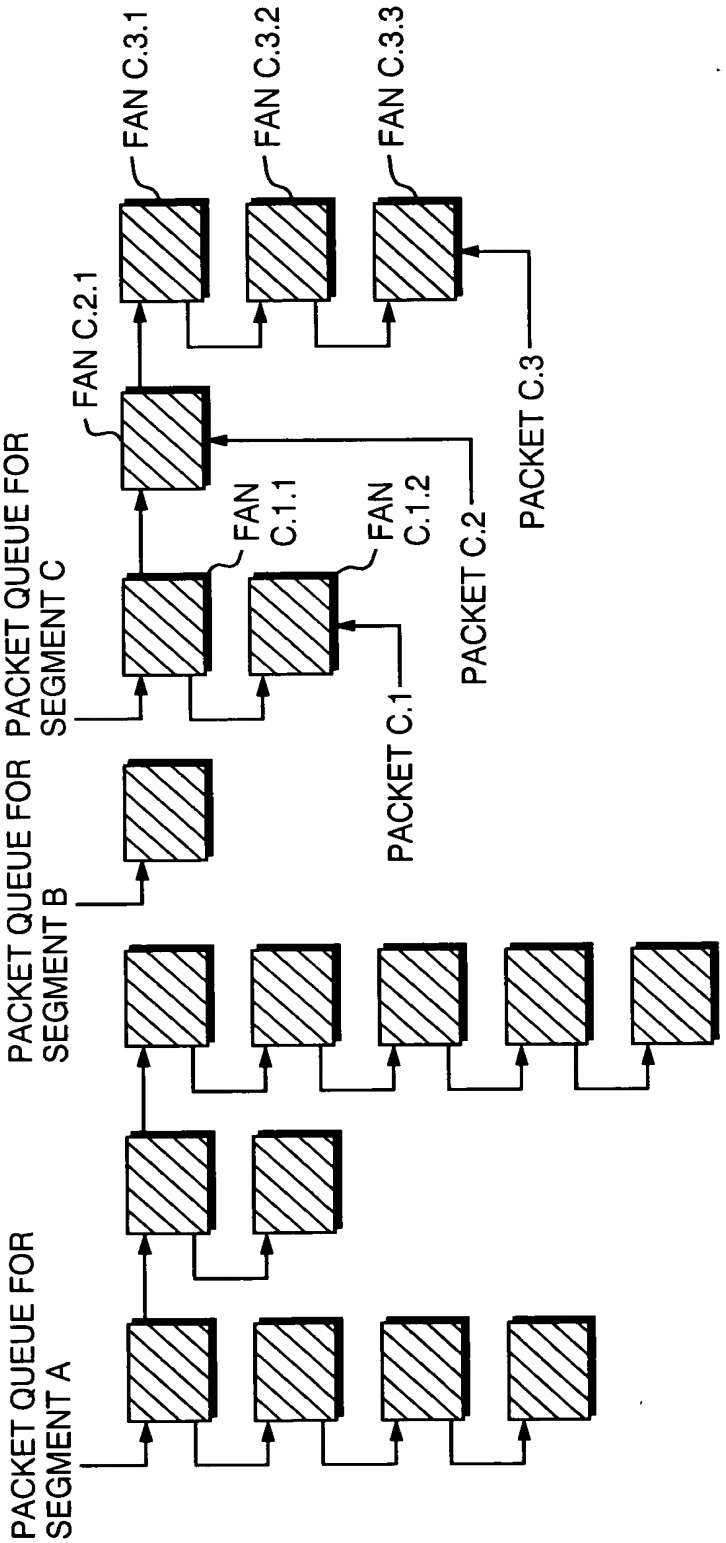
PACKET QUEUE FOR SEGMENT A
PACKET QUEUE FOR SEGMENT B
PACKET QUEUE FOR SEGMENT C
FAN C.2.1
FAN C.3.1
FAN C.3.2
FAN C.3.3
FAN C.1.1
FAN C.1.2
PACKET C.1
PACKET C.2
PACKET C.3

FIG. 14

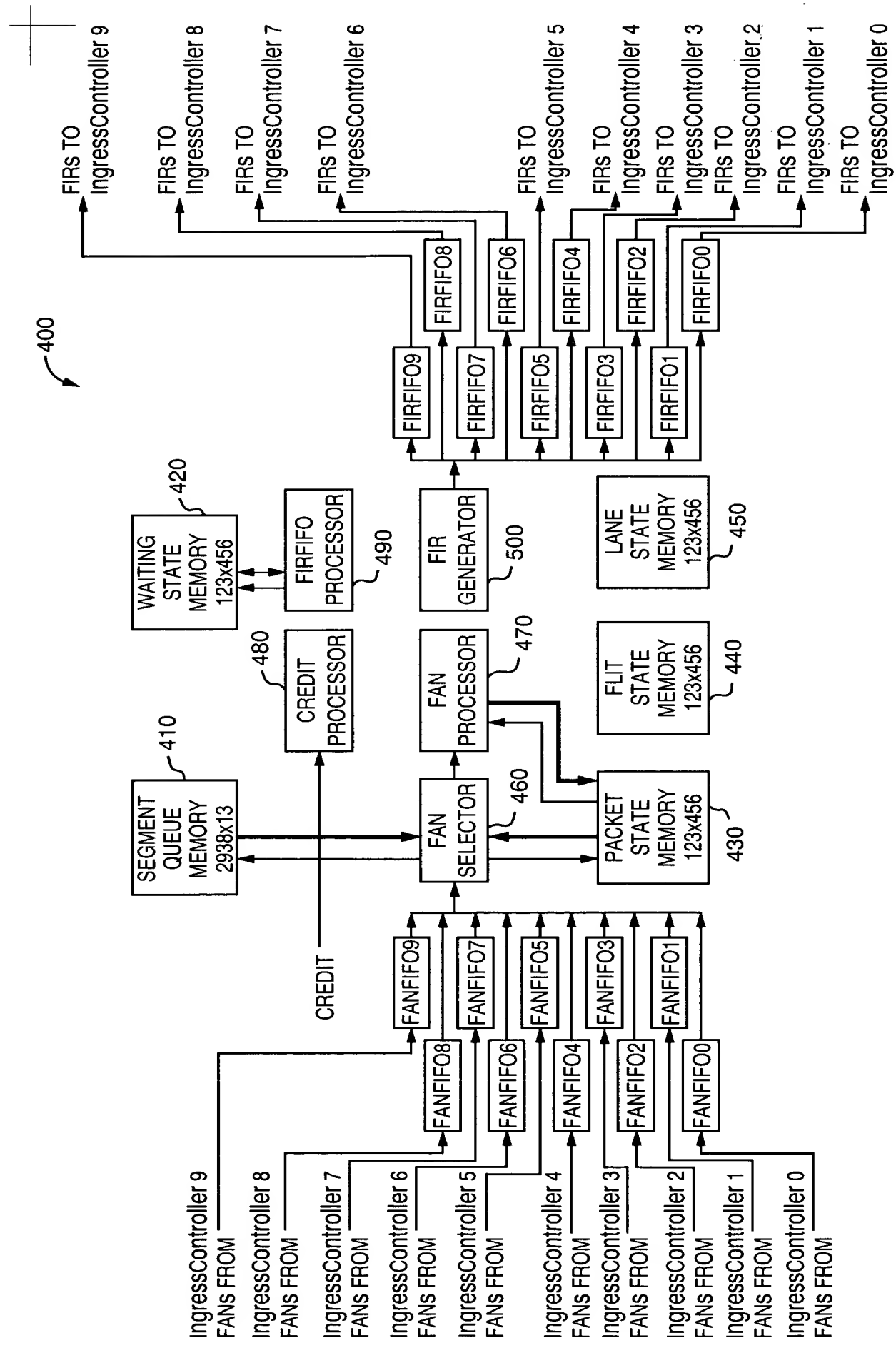
400
FIRs TO IngressController 9
FIRs TO IngressController 8
FIRs TO IngressController 7
FIRs TO IngressController 6
FIRs TO IngressController 5
FIRs TO IngressController 4
FIRs TO IngressController 3
FIRs TO IngressController 2
FIRs TO IngressController 1
FIRs TO IngressController 0
FIRFIFO9
FIRFIFO8
FIRFIFO7
FIRFIFO6
FIRFIFO5
FIRFIFO4
FIRFIFO3
FIRFIFO2
FIRFIFO1
FIRFIFO0
WAITING STATE MEMORY 123x456
420
FIRFIFO PROCESSOR
490
FIR GENERATOR
500
LANE STATE MEMORY 123x456
450
CREDIT PROCESSOR
480
FAN PROCESSOR
470
FLIT STATE MEMORY 123x456
440
SEGMENT QUEUE MEMORY 2938x13
410
FAN SELECTOR
460
PACKET STATE MEMORY 123x456
430
CREDIT
FANFIFO9
FANFIFO8
FANFIFO7
FANFIFO6
FANFIFO5
FANFIFO4
FANFIFO3
FANFIFO2
FANFIFO1
FANFIFO0
IngressController 9 FANs FROM
IngressController 8 FANs FROM
IngressController 7 FANs FROM
IngressController 6 FANs FROM
IngressController 5 FANs FROM
IngressController 4 FANs FROM
IngressController 3 FANs FROM
IngressController 2 FANs FROM
IngressController 1 FANs FROM
IngressController 0 FANs FROM

FIG. 15